WHAT IS CLAIMED IS

1. A semiconductor integrated circuit, comprising:

pads;

a first power supply I/O cell which is connected to an external pin through a corresponding one of said pads; and

a second power supply I/O cell which is not connected to an external pin through a corresponding one of said pads, but receives power supply from said first power supply I/O cell.

2. The semiconductor integrated circuit as claimed in claim 1, further comprising:

an internal cell;

a power supply line which provides power supply to said internal cell;

a line which connects between said first power supply I/O cell and said power supply line; and

a line which connects between said second power supply I/O cell and said power supply line.

3. The semiconductor integrated circuit as claimed in claim 1, wherein said second power supply I/O cell is not connected to the corresponding one of pads that corresponds to said second power supply

I/O cell.

4. A method of designing a power supply layout of a semiconductor integrated circuit, comprising the steps of:

identifying an unused I/O cell having no external connection; and

assigning the I/O cell to be a power supply I/O cell having no direct external connection.

5. The method as claimed in claim 4, further comprising a step of connecting the power supply I/O cell to a power supply line for providing power supply to an internal cell and connecting the power supply I/O cell to a power supply I/O cell having direct external connection through a pad.

6. The method as claimed in claim 4, further comprising a step of identifying a portion that is lacking in a power supply current inside a chip, wherein said step of assigning the I/O cell assigns the power supply I/O cell with respect to said portion.

7. The method as claimed in claim 6,

wherein said step of identifying a portion that is lacking in a power supply current includes the steps of:

obtaining first information about assignment of pins to I/O cells;

obtaining second information about an amount of a necessary power supply current needed at each position inside the chip;

calculating an amount of a provided power supply current in an initial state based on the first information; and

comparing the calculated amount of a provided power supply current with the amount of a necessary power supply current indicated by the second information.

8. The method as claimed in claim 4, wherein said step of assigning the I/O cell includes a step of identifying the I/O cell to be assigned by use of a pointing device on a screen display that presents an illustration of a chip.

9. The method as claimed in claim 4, wherein said step of assigning the I/O cell includes a step of identifying the I/O cell to be assigned by specifying a number that has been allocated on the chip.

10. A semiconductor integrated circuit, made by a designing process that comprises:

identifying an unused I/O cell having no external connection; and

assigning the I/O cell to be a power supply I/O cell having no direct external connection.